REMARKS

Claims remaining in the present patent application are numbered 1-27. The rejections and comments of the Examiner set forth in the Office Action dated February 11, 2004 have been carefully considered by the Applicant. Applicant respectfully requests the Examiner to consider and allow the remaining claims.

35 U.S.C. §103 Rejection

The present Office Action rejected Claims 1-27 under 35 U.S.C. 103(a) as being unpatentable over Applicant's admission of prior art (AAPA), in view of Gates (U.S. Patent No. 5,826,068). Applicant has reviewed the above cited references and respectfully submit that the present invention as recited in Claims 1-27, is neither anticipated nor rendered obvious by AAPA alone or taken in combination with the Gates reference.

Independent Claims 1 and 18

Applicant respectfully points out that currently amended independent Claims 1 and Claim 18 recite that the present invention includes, in part:

> [A] method of automatically detecting memory size comprising the steps of:
>
> a) sending a READ command from a memory controller chip to a serial peripheral interface (SPI) device over an SPI interface for a first series of eight serial clock cycles;
>
> b) driving a data Input/Output (D-IO) pin in said memory controller chip low for a second series of eight serial clock cycles;
>
> c) floating said D-IO pin after said second series of eight serial clock cycles, such that said D-IO pin is weakly pulled down in the absence of data from said SPI device and is overcome in the presence of data from said SPI device;
>
> d) automatically determining that said SPI device has memory addresses of up to nine bits when detecting the presence of

a first non-zero value coming from said SPI device through said D-IO pin during a third series of eight serial clock cycles; and

e) automatically determining that said SPI device has memory addresses of up to sixteen bits when detecting the presence of a first zero value at said D-IO pin during said third series of eight serial clock cycles and a second non-zero value coming from said SPI device through said D-IO pin during a fourth series of eight serial clock cycles.

Embodiments of the present invention pertain to the automatic detection of memory size of a serial periphery interface (SPI) device that is electrically coupled to a memory controller. In particular, independent Claim 1, as currently amended, recites that a memory controller through signals over a single data input/output (D-I/O) line can automatically determine the memory size of an SPI device that is coupled to the memory controller. Specifically, in independent Claims 1 and 18, the size of an SPI device is automatically determined by driving an D-IO pin low for a second series of eight cycles during an address phase and then floating the D-IO pin. The D-IO pin is weakly pulled down in the absence of data from the SPI device and is overcome with the presence of data from the SPI device. An SPI device having memory addresses of up to nine bits is automatically determined when the memory controller detects the presence of a non-zero value coming from the SPI device over the D-I/O pin during a third series of eight cycles. An SPI device having memory addresses of up to sixteen bits is automatically determined when the memory controller detects the presence of a zero value in the third series of eight clock cycles coming over the D-I/O pin followed by a non-zero value over the D-I/O pin in a fourth series of eight clock cycles.

Applicant respectfully notes that the Applicant's admitted prior art, taken alone or in combination with the Gates reference does not ~~comprise~~ teach nor suggest automatically determining and detecting a memory size of an SPI device by

examining when the data signals received from the SPI device over a single D-I/O pin are received, as is presently claimed in amended independent Claims 1 and 18.

It is suggested that the Gates reference suggests a series of serial clock cycles as part of a method of automatically detecting memory size. In particular, it is suggested that a series of serial clock cycles is inherent from the following text: "to said clock input line of said serial port and further . . ." (See Gates, col. 47, line 1). Also, it is similarly suggested that a series of serial clock cycles is inherent from the following text: "wherein said serial port waits for a predetermined time . . ." (see Gates, col. 47, line12). Also, it is suggested that a series of serial clock cycles is inherent from the following text: "The integrated circuit of Claim 1, wherein the duration of said predetermined time period is at least two cycles in said clock signal." Applicant respectfully asserts that the Gates reference discloses a serial port over which clock cycles of signals are detected. As such, Applicant respectfully asserts that the Gates reference does not suggest the series of 8 clock cycles of the present invention where a D-IO pin ~~is driven~~ low for a second series of 8 clock cycles; the D-IO pin is floated after the second series of 8 clock cycles; it is determined that the SPI device has a memory address of up to 9 bits when detecting non-zero values in a third series of 8 clock cycles; and it is determined that the SPI device has a memory address of up to 16 bits when detecting a zero value during the third series of eight serial clock cycles and a non-zero value during a fourth series of eight serial clock cycles.

It is suggested that the AAPA suggests first, second, third, and fourth serial clock cycles. Applicant agrees to the statement of non-admission that the prior art method does not include a series of serial clock cycles. Applicant ~~asserts that the~~ AAPA discloses that an EEPROM may vary in size and may consists of and address

nor is it taught that

or is it taught that

of one, two, three bytes or larger. That is, Applicant respectfully asserts that the AAPA does not suggest the series of 8 clock cycles of the present invention where a D-IO pin is driven low for a second series of 8 clock cycles; the D-IO pin is floated after the second series of 8 clock cycles; it is determined that the SPI device has a memory address of up to 9 bits when detecting non-zero values in a third series of 8 clock cycles; and it is determined that the SPI device has a memory address of up to 16 bits when detecting a zero value during the third series of eight serial clock cycles and a non-zero value during a fourth series of eight serial clock cycles.

?

The Applicant agrees that the cited references do not teach the automatic detection of the presence of non-zero values coming from the SPI device through the D-IO pin during a series of serial clock cycles. The Applicant also agrees that the cited references do not include an indication that the SPI device has memory addresses up to nine or sixteen bits. That is, Applicant respectfully asserts that the prior art references do not include the automatic detection between address sizes of up to nine or up to sixteen bits in an SPI device.

It is suggested that that Gates reference teaches a bi-directional pin as part of its method for automatically detecting memory size. Applicant respectfully asserts that the presence of a bi-directional pin and the disclosure of the automatic detection of the presence or absence of various predetermined devices fails to teach or suggest automatically determining and detecting a memory size of an SPI device by driving a D-IO pin low for a second series of 8 clock cycles; floating the D-IO pin after the second series of 8 clock cycles; determining that the SPI device has a memory address of up to 9 bits when detecting non-zero values in a third series of 8 clock cycles; and determining that the SPI device has a memory address of up to 16 bits when detecting a zero value during the third series of eight serial

clock cycles and a non-zero value during a fourth series of eight serial clock cycles, as presently recited in independent Claims 1 and 18.

In particular and in contrast to independent Claims 1 and 18, the Gates reference pertains to a host adapter integrated circuit that contains data transfer modules, wherein the host adapter has a serial port that uses a single serial port pin to communicate with a slave serial port input-output integrated circuit that interfaces to various resources (e.g., memory resources) that are included in a support circuit. Specifically, the Gates reference discloses an ID-ESTAT detector 1375 that senses signals over a number of high address lines, such as, the first memory address line MA17 and a second memory address line MA16, instead of the single D-IO line of claims 1 and 18 of the present invention. In particular, the ID-ESTAT detector 1375 determines that the size of EEPROM 290 is 64 kilobytes when the ID-ESTAT detector 1375 senses that a low signal on MA17 and a low signal on MA16. Further, the ID-ESTAT detector 1375 determines that the size of the EEPROM 290 is 128 kilobytes when the ID-ESTAT detector 1375 senses a high signal on MA16 and a low signal on MA17. Also, the ID-ESTAT detector 1375 determines that the size of the EEPROM 290 is 256 kilobytes when the ID-ESTAT detector 1375 senses a high signal on MA16 and a high signal on MA17. (See Figures 13 and 16, and col. 42, lines 17-22 of the Gates reference).

As such, the Gates reference discloses the presence or absence of various resources from the signals present on one or more lines connected to the resource. That is, the slave serial port input output integrated circuit 254 interfaces with various resources to distinguish between and determine the size of various resources by examining the signals over one or more lines. Thus, the automatic determination of the presence or absence of various predetermined devices is

determined at the slave serial port input output integrated circuit 254. Moreover, the transfer of information between the slave serial port input output integrated circuit 254 might occur over a single bi directional pin; however, the automatic determination of the sizes of the various resources does not occur by examining the signal over the bi-directional pin, as is recited in independent Claims 1 and 18, but is instead performed before any signals are sent to the host adapter 240 over the bi-directional pin by the slave serial port input output integrated circuit 254.

The process outlined in the Gates reference is fundamentally different from the embodiments of independent Claims 1 and 18. In particular, the Gates reference discloses the discovery of the presence or absence of multiple resources (e.g., memory devices) that are coupled to the slave serial port input output integrated circuit 254. On the other hand, embodiments of the present invention in independent Claims 1 and 18 recite the automatic determination between address sizes of a single SPI device. Moreover, the Gates reference discloses the discovery of the presence or absence of multiple resources through the examination of signals over one or more lines connected to the resource. On the other hand, embodiments of the present invention in independent Claims 1 and 18 recite the automatic determination between addresses sizes of a single SPI device by examining the signal over a single D-IO pin.

Applicant respectfully asserts that the combination of a bi-directional pin that transfers information from a host adapter to the slave serial port input-output circuit taken alone or in combination with the AAPA do not ~~comprise~~ teach nor suggest automatically determining and detecting a memory size of an SPI device by examining when the data signals received from the SPI device over a single D-I/O pin are received, as is presently recited in independent Claims 1 and 18. Even if

the AAPA discloses first, second, third, and fourth serial clock cycles, which Applicant respectfully denies, the combination of the Gates reference as well as the AAPA fail to teach or suggest the use of a series of 8 clock cycles where a D-IO pin is driven low for a second series of 8 clock cycles; the D-IO pin is floated after the second series of 8 clock cycles, such that the D-IO pin is weakly pulled down in the absence of data from the SPI device and is overcome with the presence of data from the SPI device; it is determined that the SPI device has a memory address of up to 9 bits when detecting non-zero values in a third series of 8 clock cycles; and it is determined that the SPI device has a memory address of up to 16 bits when detecting a zero value during the third series of eight serial clock cycles and a non-zero value during a fourth series of eight serial clock cycles, as recited in independent Claims 1 and 18.

Furthermore, dependent Claims 7 and 24 recite details of the SPI interface. The Gates reference taken alone or in combination with the admitted AAPA fail to teach or render obvious embodiments of the present invention as recited in dependent Claims 7 and 24. Namely, dependent Claims 7 and 24 recite that the SPI interface includes a memory controller chip with three controller pins: a serial clock pin, a chip select pin and the D-IO pin that is coupled to a serial input (SI) and serial output (SO) pins on the SPI device. The SI and SO pins are coupled to form a bidirectional signal. Also, a pull down resistor is coupled to the SI and SO pins in order to float the D-IO pin. As such, D-IO pin is pulled down in the absence of data from the SPI device and is overcome with the presence of data from the SPI device.

Also, dependent Claims 8 and 25 are not taught or rendered obvious by the Gates reference taken alone or in combination with the admitted AAPA. While

the Gates reference does mention the detection of the absence of resources, the Gates reference taken alone or in combination with the admitted AAPA fails to teach or render obvious the determination of the absence of the SPI device when zero values are detected in the third and fourth series of eight serial clock cycles over the D-IO pin, as specifically recited in dependent Claims 8 and 25.

In addition, dependent Claims 9 and 26 recite further detection of even larger memory addresses that are not taught or rendered obvious by the Gates reference taken alone or in combination with the admitted AAPA. Specifically, dependent Claims 9 and 26 recite the determination of an SPI device having memory addresses of up to 24 bits when a first zero value is detected over the D-IO line in the third series of 8 serial clock cycles, a second zero value is detected over the D-IO line in a fourth series of 8 serial clock cycles, a non-zero value is detected through the D-Io pin during a fifth series of 8 serial clock cycles with a sensing circuit.

Moreover, dependent Claims 10 and 27 recite a pulldown resistor for floating the D-IO pin that are not taught or rendered obvious by the Gates reference taken alone or in combination with the admitted AAPA. Specifically, dependent Claims 10 and 27 recite a pulldown resistor coupled to the SI pin and the SO pin of the SPI device to float the D-IO pin to a logic "0" level, such that the D-IO pin is weakly pulled down in the absence of data from the SPI device and is overcome with the presence of data from the SPI device

Thus, Applicant respectfully submits that the present embodiments as disclosed in independent Claims 1 and 18 are neither anticipated nor rendered obvious by the Gates reference, taken alone or in combination with AAPA and are

in a condition for allowance. In addition, Applicant respectfully submits that Claims 2-10 which depend from independent Claim 1 are also in a condition for allowance as being dependent on an allowable base claim. Furthermore, Applicant respectfully submits that Claims 19-27 which depend from independent Claim 18 are also in a condition for allowance as being dependent on an allowable base claim.

Independent Claim 11

As for Claims 11-17, these constitute the SPI circuit for the methods disclosed in Claims 1-10 and 18-27. The arguments set forth in relation to independent Claims 1 and 18 of the previous section are applicable to independent Claim 11. As such, Applicant argues that the combined references of Gates and the admitted AAPA do not teach or suggest the present method of automatically determining the memory size of an SPI device over a single D-IO line, as ~~found~~ claimed in independent Claim 11.

Specifically, Applicant respectfully points out that independent Claim 11 recites that the present invention includes, in part:

> [A] serial peripheral interface (SPI) circuit for automatically detecting memory size comprising:
>
> a memory controller chip comprising a first serial clock pin for providing a clock signal, a data Input/Output (D-IO) pin, and a first chip select pin for sending a chip select signal;
>
> an SPI device comprising a second serial clock pin for receiving said clock signal, a serial input pin (SI) coupled to a serial output (SO) pin, and a second chip select pin for receiving said chip select signal;
>
> a pulldown resistor coupled to said SI and SO pins;
>
> a sensing circuit for detecting data signals coming from said SPI device;

means for coupling said SPI device to said memory controller chip, said sensing circuit, and to said pulldown resistor; and
means for detecting memory size of said SPI device.

Embodiments of independent Claim 11 pertain to an SPI circuit for the automatic detection of memory size of a serial peripheral interface (SPI) device that is electrically coupled to a memory controller. In particular, independent Claim 11, recites that a memory controller includes three control pins that are used to determine the size of the SPI device: a serial clock pin, a bi-directional D-IO pin, and a chip select pin. In addition, the SPI circuit includes pulldown resistor coupled to the SI and SO pins a well as means for detecting memory size of the SPI device.

Applicant respectfully asserts that the Gates reference fails to teach or render obvious the SPI circuit as recited in independent Claim 11. That is, the Gates reference and the admitted AAPA do not teach or render obvious the memory controller chip, the SPI device, a pulldown resistor, a sensing circuit, means for coupling the memory controller chip, the sensing circuit and the pulldown resistor, and means for detecting memory size of the SPI device.

Furthermore, with regards to dependent Claim 14, Applicant respectfully asserts that the Gates reference taken alone or in combination with the admitted AAPA fail to teach or suggest the use of a series of 8 clock cycles where means for driving a D-IO pin low for a second series of 8 clock cycles is provided; means are provided for floating the D-IO pin after the second series of 8 clock cycles, such that the D-IO pin is weakly pulled down in the absence of data from the SPI device and is overcome with the presence of data from the SPI device; means are provided for determining that the SPI device has a memory address of up to 9 bits when

detecting non-zero values in a third series of 8 clock cycles; and means are provided for determining that the SPI device has a memory address of up to 16 bits when detecting a zero value during the third series of eight serial clock cycles and a non-zero value during a fourth series of eight serial clock cycles.

Moreover, with regards to dependent Claim 17, Applicant respectfully asserts that the Gates reference taken alone or in combination with the admitted AAPA fail to teach or suggest the indication the absence of the SPI device when zero values are detected in the third and fourth series of eight serial clock cycles over the D-IO pin.

As such, Applicant respectfully submits that the present invention as disclosed in independent Claim 11 is neither anticipated nor rendered obvious by the Gates reference, taken alone or in combination with the admitted prior art, and is in a condition for allowance. In addition, Applicant respectfully submits that Claims 12-17 which depend from independent Claim 11, as currently amended, are also in a condition for allowance as being dependent on an allowable base claim.

CONCLUSION

In light of the amendments and arguments presented herein, Applicant respectfully requests reconsideration of the rejected Claims.

Based on the arguments presented above, Applicant respectfully asserts that Claims 1-27 overcome the rejections of record. Therefore, Applicant respectfully solicits allowance of these Claims.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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